

DS1225Y 64k Nonvolatile SRAM

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2k x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 28-pin DIP package
- Read and write access times as fast as 150 ns
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT

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24-Pin ENCAPSULATED PACKAGE 720-mil EXTENDED

PIN DESCRIPTION

A0-A12	- Address Inputs
DQ0-DQ7	- Data In/Data Out
CE	- Chip Enable
WE	- Write Enable
ŌĒ	- Output Enable
V _{CC}	- Power (+5V)
GND	- Ground

DESCRIPTION

The DS1225Y 64k Nonvolatile SRAM is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 8k x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for micro-processor interfacing.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground **Operating Temperature** Storage Temperature Soldering Temperature Caution: Do Not Reflow

-0.3V to +7.0V 0° C to 70° C; -40°C to +85°C for IND parts -40° C to $+70^{\circ}$ C; -40° C to $+85^{\circ}$ C for IND parts +260°C for 10 seconds (Wave or Hand Solder Only)

This is a stress rating only and functional operation of the device at these or any other conditions * above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPER		(T _A : See	Note 10)			
PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V	
Input Logic 1	V _{IH}	2.2		VCC	V	
Input Logic 0	V _{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARAC	S	(T _A : See Note 10; V _{CC} = 5V ± 10%)				
PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Leakage Current	I _{IL}	-1.0		+1.0	μA	
I/O Leakage Current	т	1.0		.10		
$\overline{CE} \ge V_{IH} \le V_{CC}$	I _{IO}	-1.0		+1.0	μΑ	
Output Current @ 2.4V	I _{OH}	-1.0			mA	
Output Current @ 0.4V	I _{OL}	2.0			mA	
Standby Current $\overline{CE} = 2.2V$	1 _{CCS1}		5	10	mA	
Standby Current $\overline{CE} = V_{CC} - 0.5V$	1 _{CCS2}		3	5	mA	
Operating Current t _{CYC} =200ns (Commercial)	1 _{CCO1}			75	mA	
Operating Current t _{CYC} = 200ns (Industrial)	I _{CCO1}			85	mA	
Write Protection Voltage	V _{TP}		4.25		V	10

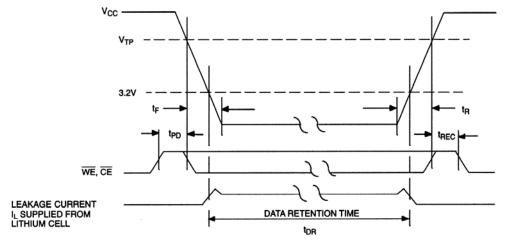
AC ELECTRICAL CHARACTERISTICS (t _A : See Note 10; $V_{CC} = 5.0V \pm 10\%$								± 10%)	
		DS1225Y-150		DS1225Y-170		DS1225Y-200			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t _{RC}	150		170		200		ns	
Access Time	t _{ACC}		150		170		200	ns	
OE to Output Valid	t _{OE}		70		80		100	ns	
$\overline{\text{CE}}$ to Output Valid	t _{CO}		150		170		200	ns	
\overline{OE} or \overline{CE} to	t _{COE}	5		5		5		ns	5
Output Active									
Output High Z from	t _{OD}		35		35		35	ns	5
Deselection									
Output Hold from	t _{OH}	5		5		5		ns	
AddressChange									
Write Cycle Time	t _{WC}	150		170		200		ns	
Write Pulse Width	t _{WP}	100		120		150		ns	3
Address Setup Time	t _{AW}	0		0		0		ns	
Write Recovery Time	t _{WR1}	0		0		0		ns	12
	t _{WR2}	10		10		10		ns	13
Output High Z from \overline{WE}	t _{ODW}		35		35		35	ns	5
Output Active from \overline{WE}	t _{OEW}	5		5		5		ns	5
Data Setup Time	t _{DS}	60		70		80		ns	4
Data Hold Time	t _{DH1}	0		0		0		ns	12
	t _{DH2}	10		10		10		ns	13

CAPACITANCE

 $(T_A = 25^{\circ}C)$

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Capacitance	C _{IN}			10	pF	
Input/Output Capacitance	C _{I/O}			10	pF	

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES			
$\overline{\text{CE}}$ at V _{IH} before Power-Down	t _{PD}	0		μs	11			
V_{CC} Slew from V_{TP} to 0V	t _F	100		μs				
V_{CC} Slew from 0V to V_{TP}	t _R	0		μs				
$\overline{\text{CE}}$ at V _{IH} after Power-Up	t _{REC}		2	ms				
					$(T_{A} = 25^{\circ}C)$			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES			
Expected Data Retention Time	top	10		vears	9			

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

- 1. WE is high for a read cycle.
- 2. $\overline{OE} = V_{IH}$ or V_{IL} . If $\overline{OE} = V_{IH}$ during a write cycle, the output buffers remain in a high impedance state.
- 3. t_{WP} is specified as the logical AND of \overline{CE} and \overline{WE} . t_{WP} is measured from the latter of \overline{CE} or \overline{WE} going low to the earlier of \overline{CE} or \overline{WE} going high.
- 4. t_{DS} is measured from the earlier of \overline{CE} or \overline{WE} going high.
- 5. These parameters are sampled with a 5 pF load and are not 100% tested.
- 6. If the \overline{CE} low transition occurs simultaneously with or later than the \overline{WE} low transition in Write Cycle 1, the output buffers remain in a high-impedance state during this period.
- 7. If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high-impedance state during this period.

- 8. If \overline{WE} is low or the \overline{WE} low transition occurs prior to or simultaneously with the \overline{CE} low transition, the output buffers remain in a high-impedance state during this period.
- 9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
- 10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
- 11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC} .
- 12. t_{WR1} , t_{DH1} are measured from \overline{WE} going high.
- 13. t_{WR2} , t_{DH2} are measured from \overline{CE} going high.
- 14. DS1225Y modules are recognized by Underwriters Laboratory (U.L.®) under file E99151 (R).

DC TEST CONDITIONS

Outputs open. All voltages are referenced to ground.

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate Input Pulse Levels: 0-3.0V Timing Measurement Reference Levels Input:1.5V Output: 1.5V Input Pulse Rise and Fall Times: 5ns

PART NUMBER	TEMPERATURE RANGE	SUPPLY TOLERANCE	PIN/PACKAGE	SPEED GRADE
DS1225Y-150	0° C to $+70^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	150ns
DS1225Y-150+	0° C to $+70^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	150ns
DS1225Y-150IND	-40°C to +85°C	$5V \pm 10\%$	28 / 720 EMOD	150ns
DS1225Y-150IND+	-40°C to +85°C	$5V \pm 10\%$	28 / 720 EMOD	150ns
DS1225Y-170	0° C to $+70^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	170ns
DS1225Y-170+	0° C to $+70^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	170ns
DS1225Y-200	0° C to $+70^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	200ns
DS1225Y-200+	0° C to $+70^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	200ns
DS1225Y-200IND	-40° C to $+85^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	200ns
DS1225Y-200IND+	-40° C to $+85^{\circ}$ C	$5V \pm 10\%$	28 / 720 EMOD	200ns

ORDERING INFORMATION

+ Denotes lead-free/RoHS-compliant product.